IN THE CLAIMS

Please cancel claims 1-26 without prejudice.

Please add new claims 27-57 as follows:

27. (New) A rewiring substrate strip comprising:

a rewiring substrate having several semiconductor component positions configured for semiconductor components, wherein the component positions are arranged in rows and columns; and

a component group defined by several semiconductor component positions configured to arrange semiconductor components located in the several semiconductor component positions with respect to one another such that an individual semiconductor component is rotated by substantially 90 degrees or 270 degrees with respect to four adjacent semiconductor components.

28. (New) The rewiring substrate strip of claim 27, comprising:

a semiconductor component located in each semiconductor component position.

29. (New) The rewiring substrate of claim 27, comprising wherein the semiconductor component positions are configured to arrange semiconductor components positioned therein in a parquet pattern.

30. (New) The rewiring substrate of claim 27, comprising:

cutting strips within a component group, bounded by cutting lines and comprise test contact surfaces between the rows and columns.

31. (New) A rewiring substrate strip comprising:

a plurality of semiconductor component positions for semiconductor components that are arranged in semiconductor chips arranged in several component rows and component columns subdivided by cutting lines;

wherein several semiconductor components positions are combined to form one component group, the component group comprising several semiconductor chips of the semiconductor components on a top side of the rewiring substrate strip; and

wherein cutting strips which have test contact surfaces are provided between the component rows and component columns within a component group, the semiconductor component positions and the test contact surfaces being aligned with respect to one another in such a manner that a parqueting pattern according to a parallel-rod Parquet pattern is produced and the arrangements of external contacts and test contact surfaces on a rear side of the rewiring substrate strip are correspondingly aligned with respect to one another in such a manner that the arrangements of four next neighbors of a semiconductor component are rotated by uniformly 90° or by uniformly 270° with respect to the one arrangement in accordance with a predetermined plan.

32. (New) The rewiring substrate strip according to claim 31, comprising:

wherein the component rows and component columns comprise first and second semiconductor chips, the first and second semiconductor chips differing in their alignments and the first semiconductor chips having a first alignment and the second semiconductor chips having a second alignment rotated uniformly by 90° or uniformly by 270° with respect to the first alignment A, and the first and second semiconductor chips being arranged alternately in the component rows and component columns.

33. (New) The rewiring substrate strip according to claim 31, comprising:

wherein on a rear side, opposite to the top side, of the rewiring substrate strip external contact patches having external contacts are arranged in the semiconductor component

positions and wherein the external contact patches are electrically connected to the test contact surfaces on the cutting strips via rewiring lines.

34. (New) The rewiring substrate strip according to claim 31, comprising:

where in the semiconductor component positions, the test contact surfaces on cutting strip sections which are arranged at two opposite edges of the semiconductor components are allocated to the respective semiconductor component position.

35. (New) The rewiring substrate strip according to claim 31, comprising:

wherein the cutting strips are arranged horizontally along the component rows and vertically along the component columns, and in each case form an intersection area which comprises a number of test contact surfaces, a quarter of these test contact surfaces on an intersection area in each case being allocated to one of the four adjoining semiconductor component positions.

36. (New) The rewiring substrate strip according to claim 31, comprising wherein one or more component groups are arranged in a row behind one another and/or next to one another on the rewiring substrate strip and preferably have one or more plastic covers.

37. (New) The rewiring substrate strip according to claim 31, comprising where in the semiconductor component positions, external contact patches having external contacts are arranged in an external contact patch matrix with external contact rows and external contact columns.

38. (New) The rewiring substrate strip according to claim 31, comprising wherein the semiconductor chips are electrically connected to the rewiring substrate strip via flip chip contacts or via bonding wire connections.

39. (New) The rewiring substrate strip according to claim 31, comprising wherein the rewiring substrate strip has on its rear side, outside the area of a component group, areas with exposed test contact surfaces, the test contact surfaces being electrically connected to the test contact surfaces in the cutting strips and/or the external contact patches of the semiconductor components via rewiring lines.

40. (New) The rewiring substrate strip according to claim 31, comprising wherein the rewiring substrate strip has in an edge area a plug-in contact strip with plug-in contact surfaces, the plug-in contact surfaces being electrically connected to the test contact surfaces and/or to test contact surfaces and/or the external contact patches.

41. (New) The rewiring substrate strip according to claim 40, comprising wherein the plug-in contact strip of the rewiring substrate strip is provided for a temperature cycle test or, respectively, "burn-in" test.

42. (New) The rewiring substrate strip according to claim 31, comprising wherein the test contact surfaces carry test contacts.

43. (New) The rewiring substrate strip according to claim 31, comprising wherein the test contact surfaces comprise gold plating.

44. (New) The rewiring substrate strip according to claim 31, comprising wherein the rewiring substrate strip has in the semiconductor component positions stacks of a logic chip and a memory chip, wherein both the memory functions of the memory chip and the logic functions of the logic chip can be tested via test contact surfaces and/or via exposed test contact surfaces and/or via test contacts and/or via plug-in contact strips.

45. (New) A semiconductor component comprising:

a rewiring substrate strip comprising:

a rewiring substrate having several semiconductor component positions configured for semiconductor components, wherein the component positions are arranged in rows and columns, and a component group defined by several semiconductor component positions configured to arrange semiconductor components located in the several semiconductor component positions with respect to one another such that an individual semiconductor component is rotated by substantially 90 degrees or 270 degrees with respect to four adjacent semiconductor components;

a semiconductor component located in each semiconductor component position; and

wherein the rewiring substrate strip is separated to comprise on opposite edges cut rewiring lines which led to test contact surfaces on cutting strips of the rewiring substrate strip.

46. (New) A method for producing a rewiring substrate strip with several component groups, wherein the component groups comprise semiconductor component positions with semiconductor chips, the semiconductor component positions being arranged in component rows in the x-direction and in component columns in the y-direction, wherein the method comprises:

providing a substrate strip which is metal-plated on its rear side;

applying a rewiring structure on the metal-plated substrate strip, the rewiring structure comprising external contact patches in the semiconductor component positions and test contact surfaces in the area of cutting strips between the semiconductor component positions;

mounting semiconductor chips on the top side of the rewiring substrate strip in the semiconductor component positions, in such a manner that first each odd-numbered semiconductor component position in the component rows and component columns is equipped with a first semiconductor chip in a first alignment and then the remaining even-

numbered semiconductor component positions are equipped with a second semiconductor chip in a second alignment which is rotated uniformly by 90° or uniformly by 270° with respect to the first alignment, so that a rod-Parquet pattern is formed in accordance with a predetermined plan in the x- and y-direction;

producing connections between the semiconductor chips and the rewiring structure;

applying external contacts in the semiconductor component positions to the external contact patches of the rewiring structure on the rear side of the rewiring substrate strip;

performing functional tests of the semiconductor chips, combined into component groups, by contacting the test contact surfaces; and

marking defective semiconductor components on the rewiring substrate strip.

47. (New) The method according to claim 46, comprising wherein the semiconductor chips are mounted uniformly and with standard alignment on the top side of the rewiring substrate strip and a rewiring structure is provided on the rewiring lines which provides in the semiconductor component positions of the rewiring substrate strip an alignment of the arrangement of external contacts which is rotated uniformly by 0° and/or 180° for odd-numbered semiconductor component positions with respect to the alignment of the semiconductor chips in the component rows and the component columns and rotated uniformly by 90° and/or uniformly by 270° with respect to the alignment of the semiconductor chips for even-numbered semiconductor component positions, so that the predetermined rotation in the semiconductor component positions is carried out by means of a predetermined redistribution plan for a multi-layered rewiring substrate strip.

48. (New) The method according to claim 47, comprising wherein for mounting differently aligned and arranged semiconductor chips on the rewiring substrate strip, a wafer separated into semiconductor chips is available which comprises semiconductor chips aligned

and arranged in a preparatory manner in an x- and y-arrangement and in rotational alignment, which are mounted on the top side of the rewiring substrate strip in this predetermined arrangement and alignment of the wafer by an automatic insertion machine.

49. (New) The method according to claim 48, comprising wherein for mounting differently aligned and arranged semiconductor chips on the rewiring substrate strip, a foil with semiconductor chips is available which comprises semiconductor chips aligned and arranged in a preparatory manner in the x- and y-arrangement and in rotational alignment, which are mounted on the top side of the rewiring substrate strip in this predetermined arrangement and alignment by an automatic insertion machine.

50. (New) The method according to claim 49, comprising wherein for mounting differently aligned and arranged semiconductor chips on the rewiring substrate strip, an automatic insertion machine which is programmable in x-, y-arrangement and rotational alignment, is used which picks up semiconductor chips arranged in standard manner and uniformly aligned from a wafer separated into semiconductor chips or from a foil uniformly equipped with semiconductor chips and which carries out the provided arrangement and alignment plan according to program during the equipping of the rewiring substrate strip.

51. (New) The method according to one of claim 50, comprising wherein the semiconductor chips in the component groups are semiconductor chips with flip chip contacts and connections between semiconductor chips and a rewiring structure are established on the top side of the rewiring substrate strip by means of a soldering process.

52. (New) The method according to one of claim 51, comprising wherein the semiconductor chips are mounted with their rear sides on the semiconductor component positions and connections between semiconductor chips and a rewiring structure on the top side of the rewiring substrate strip are established by means of bonding technology.

53. (New) The method according to one of claim 52, comprising wherein after the connections are established between semiconductor chips and rewiring substrate strip, plastic covers are applied to the component groups which embed the semiconductor chips in a plastic compound.

54. (New) The method according to one of claims 53, comprising wherein the test contact surfaces and/or the external contact patches of the rewiring structure are selectively plated with a gold alloy.

55. (New) The method according to one of claim 54, comprising wherein solder balls are soldered to the test contact surfaces as test contacts.

56. (New) A method for producing semiconductor components comprising:

producing a rewiring substrate strip comprising:

a rewiring substrate having several semiconductor component positions configured for semiconductor components, wherein the component positions are arranged in rows and columns; and

a component group defined by several semiconductor component positions configured to arrange semiconductor components located in the several semiconductor component positions with respect to one another such that an individual semiconductor component is rotated by substantially 90 degrees or 270 degrees with respect to four adjacent semiconductor components separating the rewiring substrate strip into individual components; and

sorting out the semiconductor components marked as defective.

57. (New) A rewiring substrate strip comprising:

means for providing a rewiring substrate having several semiconductor component positions configured for semiconductor components, wherein the component positions are arranged in rows and columns; and

means for providing a component group defined by several semiconductor component positions configured to arrange semiconductor components located in the several semiconductor component positions with respect to one another such that an individual semiconductor component is rotated by substantially 90 degrees or 270 degrees with respect to four adjacent semiconductor components.